T0 and T2, the FREEZE-0 is HIGH. At time T2, the EN_PSA-0 signal is activated HIGH. After a predetermined delay time caused by delay 412, indicated by D0 in Figure 5, the input of NOR gate 410-0 connected to delay 412 will be HIGH. This forces a LOW to the signal at the output of NOR gate 410-0 or the FREEZE-0 signal. If BANK-0 is the only bank that is selected in the ACTIVE mode, the STOP_PD signal would be LOW or deactivated after time T2+D0 because the FREEZE-0 signal is LOW after time T2 + D0 . However, after time T2+D0, the [B_ACT-1] B_ACT-1* signal is LOW indicating BANK-1 is still selected. Therefore, the STOP_PD signal is still forced HIGH. The STOP_PD signal is deactivated when all of the banks are not selected in the ACTIVE mode and after a predetermined time the EN_PSA signal of the last bank is activated.

The paragraph beginning at page 14, line 18 is amended as follows:

It is understood that in the test mode, the ACTIVE, READ and REFRESH modes can be simulated to determine the effect of these modes on the DLL. The simulation can be achieved by giving the right combinations of input signals on input lines such as lines 114 and 108 of memory device 100 shown in Figure 1. Because the TM_CKE signal can be controlled during the test mode to activate or deactivate the STOP_PD signal during the test mode, the effect of the simulated ACTIVE, READ or REFRESH mode on the DLL during the test can also be monitored. For example, during a the test mode the TM_CKE signal can be activated or deactivated by toggling [it] its signal levels between HIGH and LOW to activate or deactivate the STOP_PD signal. One way to observe the effect of the simulated ACTIVE, READ or REFRESH mode on the DLL is to record and compare the signal relationship between the XCLK signal and the DQ signal before and after the TM_CKE or the STOP_PD signal is activated during the test mode.

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